

GLITCH-FREE RECEIVERS FOR BI-DIRECTIONAL, SIMULTANEOUS DATA BUS

Abstract of the Disclosure

A structure and method for eliminating glitches at the output of a receiver receiving signals sent to one end of a bi-directional, simultaneous transmission line. The receiver comprises two comparators, a logic circuit, a glitch detector, and a programmable delay unit. The two comparators convert a three-state digital signal on the transmission line into two two-state digital signals so that the logic circuit can understand. When a glitch occurs at the output of the logic circuit, also the output of the receiver, caused by the transitions on the output of one of the comparators and a first signal being sent to the other end of the transmission line reaching the logic circuit not at the same time, the glitch detector causes the programmable delay unit to adjust delay to the propagation path of the first signal to the logic circuit so as to eliminate the cause of the glitch.